VOLTAGE REGULATOR USING A MULTI-POWER AND GAIN-BOOSTING TECHNIQUE AND MOBILE DEVICES INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. §119(e) to U.S. Provisional Patent Application No. 62/221,849 filed on Sep. 22, 2015, and under 35 U.S.C. §119(a) to Korean Patent Application No. 10-2015-0181279 filed on Dec. 17, 2015, the disclosures of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

[0002] Exemplary embodiments of the inventive concept relate to a voltage regulator, and more particularly, to a voltage regulator using multi-power and gain-boosting techniques and mobile devices including the same.

DISCUSSION OF RELATED ART

[0003] A mobile device can be operated for an extended period of time without having to recharge its battery due to increases in battery efficiency.

[0004] A mobile device may include a low-dropout (LDO) regulator. The LDO regulator receives an operating voltage from a power management integrated circuit (IC) included in the mobile device and converts the operating voltage into a voltage used by a semiconductor chip included in the mobile device. The LDO regulator secures a dropout voltage, e.g., a difference between an input voltage and an output voltage, to correctly generate the output voltage.

[0005] However, when the dropout voltage is too small, the overall feedback loop gain of the LDO regulator decreases. As a result, a large error occurs in the output voltage of the LDO regulator.

[0006] When an LDO regulator is supplied with a power voltage from a power management IC through power lines, an input voltage of the LDO regulator may not equal an output voltage of the power management IC. This is so, because of a voltage drop of the power lines. Accordingly, as the input voltage of the LDO regulator decreases, a dropout voltage approaches 0. In this case, the overall feedback loop gain of the LDO regulator is so low that the LDO regulator may not operate normally.

SUMMARY

[0007] According to an exemplary embodiment of the inventive concept, there is provided a voltage regulator including an error amplifier configured to receive a first voltage through a first node as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage; a power transistor connected between a second node through which a second voltage is supplied and an output node; and a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal.

[0008] According to an exemplary embodiment of the inventive concept, there is provided a mobile device including a voltage regulator and a power management integrated circuit configured to supply a first voltage to the voltage regulator through a first transmission line and to supply a second voltage to the voltage regulator through a second transmission line. The voltage regulator includes an error amplifier configured to receive the first voltage through a first node connected to the first transmission line as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage; a power transistor connected between a second node connected to the second transmission line and an output node of the voltage regulator; and a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal.

[0009] According to an exemplary embodiment of the inventive concept, there is provided a mobile device including a memory, a memory controller including a voltage regulator, and a power management integrated circuit configured to supply a first voltage and a second voltage to the voltage regulator and to supply a third voltage to the memory. The voltage regulator includes an error amplifier configured to receive the first voltage through a first node as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage; a power transistor connected between a second node receiving the second voltage and an output node of the voltage regulator; and a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal. The first voltage may be higher than the second voltage.

[0010] According to an exemplary embodiment of the inventive concept, there is provided a power transistor configured to output an output voltage of the voltage regulator; and a switch circuit configured provide a first voltage or a second voltage to a gate of the power transistor in response to at least one control signal and a level of each of the first and second voltages, and to provide the first voltage or the second voltage to a body of the power transistor in response to the at least one control signal and the level of each of the first and second voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The above and other features of the inventive concept will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[0012] FIG. **1** is a block diagram of an integrated circuit (IC) according to an exemplary embodiment of the inventive concept;

[0013] FIG. **2** is a diagram of a first switch circuit illustrated in FIG. **1** according to an exemplary embodiment of the inventive concept;

[0014] FIG. **3** is a diagram of a power selector circuit illustrated in FIG. **2** according to an exemplary embodiment of the inventive concept;